Previous Doc Next Doc Go to Doc#
First Hit Fwd Refs

Generate Collection

L6: Entry 1 of 1 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6515987 B1
TITLE: Serial to parallel conversion of data to facilitate sharing a single buffer among multiple channels

Brief Summary Text (30):
A receiver in accordance with the invention includes at least one memory, each memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal and outputs the stored data samples from a plurality of channels in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; and an outer decoder, responsive to data blocks with each data block containing at least one data group, which decodes the data blocks and outputs decoded data blocks. A pair of data processing paths is provided with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, the pair of data processing paths each containing one of the at least one memory. The soft decision processing path further comprises upstream of one of the at least one memory, another memory including an addressable storage array which stores a sequence of data samples contained in the time division multiplexed signal and outputs the stored data samples in a sequence of the data groups, each data group containing a plurality of samples from one of the plurality of channels and an inner decoder, responsive to the data groups, which decodes the data samples within the data groups and outputs the decoded data samples to the memory in the soft decision processing path. The data samples inputted to the another memory each comprise orthogonally encoded data; and the inner decoder is a biorthogonal decoder. The inner decoder is a Reed-Muller decoder. The receiver is contained in a satellite. The receiver further includes a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the channels comprising the time division multiplexed signal. The memories each further comprise a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator. The another memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the another memory with addresses generated by the write address generator and the sequence of data groups outputted from a group of memory cells of the another memory with addresses generated by the read address generator.

Brief Summary Text (31):
A method of data reception in accordance with the invention includes storing in at least one memory a received time division multiplexed signal containing a sequence of data samples from a plurality of channels; from the at least one memory outputting the stored data samples in a sequence of data groups with each data

group containing a plurality of samples from one of the plurality of channels; decoding with an outer decoder the data samples within data blocks with each data block containing at least one data group; and outputting the decoded data samples of the plurality of data blocks. A pair of data processing paths are provided with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, and wherein each data processing path contains one of the at least one memory, each memory storing a received time division multiplexed signal containing a sequence of data samples from the plurality of channels, outputting from each memory the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels, decoding the data samples within the data blocks each containing at least one data group, and outputting the decoded data samples. The soft decision path contains another memory, upstream of the memory, which stores a sequence of the data samples and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; the data group is decoded with an inner decoder; and the data decoded by the inner decoder is outputted to the memory of the soft decision processing. The data samples inputted to the another memory each comprise orthogonally encoded data; and the inner code decoder is a biorthogonal data encoder. The method is performed within a satellite. An input bandwidth is divided with a channelizer into a plurality of output channels each having an equal bandwidth, one of the output channels comprising the time division multiplexed signal. Memory cells of each of the at least one memory are addressed by addresses generated by a read address generator and a write address generator with the sequence of data samples being written in a data group of memory by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

Detailed Description Text (8):
A pair of multiple channel data converters 118 and 120 of similar construction respectively process the multiple bit outputs from the inner decoder 116 and from the data demultiplexing and reordering memory 114 to output words having a word length from one channel which the outer decoder 102 is designed to decode. The difference in the processing between the multiple channel nibble to byte converter 118 and the dibit to byte converter 120 is that the number of TDM input bits to the nibble to byte converter is four and the number of TDM input bits to the dibit byte converter is two with both converters producing a byte output. It should be understood that the processing performed by the converters 118 and 120 is not limited by any number of bits. The converters 118 and 120 convert data of multiple channels into larger data groups which are sized to facilitate efficient decoding by the outer decoder 102 which decodes data from a single channel during each decoding cycle. As a result, the number of converters required to process data with the present invention is reduced by a factor of the number of TDM channels in the data stream outputted by the phase tracking function 112.

Detailed Description Text (14):
The processing of N BIT HARD DECISIONS requires only one data conversion of N BIT HARD DECISIONS from multiple channels which is performed by converter 120 while the processing performed by the N BIT SOFT DECISIONS from multiple channels requires sequential data conversions. The sequential data conversions are performed by the data demultiplexing and reordering memory 114 which packs two-bit symbols into bytes, which are decoded by the inner decoder 116 into an output nibble of the most likely bits from multiple TDM channels, which require further conversion by the nibble to byte converter 118 to output data words from multiple TDM channels of the correct length for decoding by the outer decoder 102.

CLAIMS:

1. A receiver comprising: a pair of data processing paths with one of the data

processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path; first and second memories, connected in the soft decision processing path and the hard decision processing path, respectively, each memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal and outputs the stored data samples from a plurality of channels in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; wherein the soft decision processing path further comprises upstream of the first memory, another memory including an addressable storage array which stores a sequence of data samples contained in the time division multiplexed signal and outputs the stored data samples in a sequence of the data groups, each data group containing a plurality of samples from one of the plurality of channels and an inner decoder, responsive to the data groups, which decodes the data samples within the data groups and outputs the decoded data samples to the first memory in the soft decision processing path; a block buffer memory coupled to receive data groups from a selected one of the soft decision processing path and the hard decision processing path; and a single outer decoder coupled to receive data blocks of multichannel data from the block buffer memory, with each data block containing at least one data group, wherein the outer decoder decodes the data blocks and outputs decoded data blocks.

12. A method of data reception comprising: storing in first and second memories a received time division multiplexed signal containing a sequence of data samples from a plurality of channels; providing a pair of data processing paths with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, and wherein the hard decision data processing path and the soft decision processing path contain the first and second memories, respectively, each of the first and second memories storing a received time division multiplexed signal containing a sequence of data samples from the plurality of channels, wherein the soft decision path contains another memory, upstream of the second memory, which stores a sequence of the data samples and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels, and wherein each data group is decoded with an inner decoder, and wherein the decoded data decoded by the inner decoder is output to the second memory in the soft decision processing path; outputting from the first and second memories the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; inputting the sequence of data groups from the a selected one of the first and second memories into a block buffer memory; outputting data blocks of multichannel data into a single outer decoder, decoding with the outer decoder the data samples within data blocks with each data block containing at least one data group; and outputting the decoded data samples of the plurality of data blocks.

Previous Doc Next Doc Go to Doc#